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Original Article

Neural architecture search for optimizing edge computing in IoT devices

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ABSTRACT

The proliferation of Internet of Things (IoT) devices has intensified the demand for efficient and accurate deep learning models capable of operating under stringent resource constraints at the edge. Neural Architecture Search (NAS) offers a promising avenue to automate the design of optimized neural networks tailored for edge computing environments. This paper investigates the application of NAS for optimizing neural network architectures deployed on IoT edge devices, balancing accuracy, latency, and energy efficiency. We propose a multi-objective NAS framework that incorporates hardware-aware constraints specific to typical IoT edge platforms. Experimental results on benchmark datasets demonstrate that NAS-generated models outperform conventional architectures in terms of inference speed and power consumption, while maintaining competitive accuracy. Our findings highlight the potential of NAS as a vital tool for enhancing edge intelligence in IoT systems.

KEYWORDS

Neural Architecture Search (NAS), Edge Computing, Internet of Things (IoT), Model Optimization, Resource-Constrained Devices, Hardware-aware NAS, Energy Efficiency, Deep Learning.

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1. INTRODUCTION

1.1. Background on IoT and Edge Computing

The Internet of Things (IoT) refers to the vast network of interconnected devices embedded with sensors, software, and communication capabilities, enabling them to collect and exchange data. With billions of IoT devices deployed worldwide across industries such as healthcare, manufacturing, transportation, and smart cities, the volume of generated data is growing exponentially. This rapid proliferation has created a pressing demand for real-time data processing and analytics to enable intelligent decision-making at or near the source of data generation. Edge computing has emerged as a critical paradigm to meet this need by pushing computation closer to the devices themselves, rather than relying solely on centralized cloud servers. By processing data locally on edge devices or nearby edge servers, edge computing reduces the latency involved in transmitting data to the cloud and alleviates network bandwidth usage. This approach is particularly valuable for latency-sensitive applications like autonomous vehicles, industrial automation, and health monitoring, where delays can lead to significant performance degradation or safety risks.

1.2. Challenges in Deploying Deep Learning Models on IoT Edge Devices

Despite the benefits of edge computing, deploying deep learning models on IoT edge devices presents several unique challenges. Edge devices often have severely limited computational resources, including constrained CPU capabilities, minimal memory, and limited storage. Unlike cloud servers, which can support large and complex models, edge devices must run inference within these tight hardware limits. Moreover, many IoT devices operate on batteries or have strict energy consumption requirements, making power efficiency a critical concern. Running deep neural networks can quickly drain battery life, making the deployment of traditional large models impractical. Additionally, edge applications typically require low-latency inference to ensure timely responses, which further restricts the complexity and size of deployable models. These combined constraints necessitate the design of lightweight yet accurate neural network architectures specifically tailored for edge environments.

1.3. Motivation for Using Neural Architecture Search (NAS)

Designing efficient neural network architectures that meet the resource and performance requirements of edge devices is a complex and time-consuming task. Traditional manual architecture design involves extensive experimentation and expert intuition to strike a balance between accuracy, computational cost, and latency. However, such handcrafted models may not be optimal for the diverse and evolving landscape of edge hardware. Neural Architecture Search (NAS) offers a promising solution by automating the design process through algorithmic exploration of a predefined search space of model architectures. NAS algorithms can systematically discover architectures that are specifically optimized for target hardware constraints, such as limited memory, low computational power, and energy budgets. By incorporating hardware-awareness into the search objectives, NAS can effectively balance multiple performance metrics, including accuracy, inference speed, and power consumption, often outperforming

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manually designed models. This makes NAS a powerful tool for addressing the challenges of deploying deep learning on IoT edge devices.

1.4. Contributions of the Paper

In this paper, we present a comprehensive NAS framework tailored for optimizing neural network architectures on IoT edge devices. Our approach incorporates hardware constraints and performance trade-offs into the architecture search process, enabling the automatic discovery of models that are well-suited for resource-constrained environments. We analyze how the proposed NAS framework effectively balances model accuracy with latency and energy consumption, addressing the critical needs of edge computing applications. To validate our approach, we implement and evaluate the generated architectures on typical IoT hardware platforms, demonstrating significant improvements in inference efficiency without sacrificing predictive performance. Through extensive experiments and analysis, this paper contributes valuable insights into the potential of NAS to advance edge intelligence and provides practical guidelines for deploying optimized neural networks in real-world IoT scenarios.

2. RELATED WORK

2.1. Edge Computing in IoT

Edge computing is an emerging paradigm that shifts data processing and computation closer to the physical location where data is generated, rather than relying on centralized cloud servers. In the context of IoT ecosystems, where massive volumes of data are continuously produced by distributed devices such as sensors, cameras, and actuators, edge computing plays a crucial role in reducing the latency and bandwidth challenges associated with transmitting data to distant data centers. This localized processing enables faster response times and real-time analytics, which are vital for applications requiring immediate decision-making like autonomous vehicles, industrial control systems, and healthcare monitoring. The significance of edge computing within IoT lies in its ability to improve system scalability, enhance privacy by keeping sensitive data local, and reduce network congestion, thereby making IoT solutions more robust and efficient.

Typical hardware platforms used for edge computing vary widely depending on the application requirements and resource availability. Low-power microcontrollers (MCUs) are common in highly constrained environments, providing basic computational capabilities with minimal energy consumption. For more demanding tasks, single-board computers (SBCs) such as the Raspberry Pi or NVIDIA Jetson Nano offer higher processing power and support more sophisticated machine learning models while still operating at the network edge. These hardware platforms differ significantly in their computational resources, memory capacity, and energy efficiency, making it essential to design and optimize deep learning models that align well with the specific constraints and capabilities of the deployed devices.

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2.2. Model Optimization Techniques for Edge Devices

Deploying deep learning models on edge devices requires careful optimization to address hardware constraints without severely compromising model performance. Two widely adopted techniques are pruning and weight quantization. Pruning involves removing redundant or less important connections within neural networks, thereby reducing model size and computational overhead. Weight quantization, on the other hand, reduces the precision of the model parameters (weights) from floating-point to lower-bit representations such as 8-bit integers. This not only decreases the memory footprint but also accelerates inference through more efficient arithmetic operations, often with only marginal losses in accuracy.

Besides these, researchers have developed specialized lightweight architectures designed explicitly for resource-limited environments. MobileNet and ShuffleNet are prime examples that utilize efficient building blocks such as depthwise separable convolutions and channel shuffling to minimize computational cost and model size while maintaining reasonable accuracy. Other compression and acceleration techniques include knowledge distillation, which transfers knowledge from a large, complex model to a smaller one, and hardware-specific optimizations that tailor models to exploit parallelism or specialized instruction sets. While these techniques have shown promise, they often rely on manual tuning or heuristics, limiting their adaptability to diverse hardware configurations.

2.3. Neural Architecture Search (NAS)

Neural Architecture Search (NAS) has emerged as a powerful method to automate the design of neural network architectures, relieving researchers and engineers from the tedious and heuristic-driven process of manual model crafting. NAS explores a predefined search space of candidate architectures using optimization algorithms to identify models that best meet specific performance criteria. Common methodologies include reinforcement learning, where an agent iteratively proposes architectures and learns to improve its proposals based on reward signals; evolutionary algorithms that mimic natural selection by evolving a population of architectures over generations; and gradient-based search techniques that leverage continuous relaxation of the architecture space for efficient optimization.

NAS has achieved remarkable success in automating architecture design, especially in cloud and server environments where computational resources are abundant. For instance, NAS has been used to design state-of-the-art models that outperform human-designed counterparts on benchmarks like ImageNet. These achievements demonstrate NAS's ability to discover novel and highly optimized architectures, but they often come with high computational costs and focus on maximizing accuracy without considering resource constraints critical for edge devices.

2.4. NAS for Edge and Resource-Constrained Environments

Recognizing the limitations of traditional NAS methods for edge deployment, recent research has shifted towards hardware-aware NAS approaches that explicitly consider latency, energy consumption,

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memory footprint, and other constraints during the search process. These methods integrate hardware performance metrics into the objective function or use proxy measurements to guide the search towards architectures that can be realistically deployed on specific edge devices. For example, latency-aware NAS incorporates the inference time of candidate architectures on target hardware as a key optimization goal, balancing it against accuracy to find efficient models.

In the context of IoT and embedded devices, several advances have tailored NAS algorithms to address the unique challenges of these environments. Techniques such as multi-objective optimization, where accuracy is traded off against resource usage, and hardware-in-the-loop NAS, which evaluates architectures directly on edge devices, have shown promising results. However, despite these developments, existing literature still faces challenges related to the diversity of IoT hardware, the high cost of search procedures on constrained devices, and the need for generalizable NAS frameworks adaptable to various edge scenarios. This paper aims to fill these gaps by proposing a NAS framework that not only targets typical IoT edge platforms but also provides comprehensive insights into the trade-offs between accuracy and resource consumption, enabling more effective deployment of deep learning at the edge.

3. PROBLEM DEFINITION AND OBJECTIVES

3.1. Definition of Optimization Goals for IoT Edge Devices (Latency, Accuracy, Energy Efficiency)

In the context of deploying deep learning models on IoT edge devices, optimization must be approached as a multi-faceted objective rather than a single metric improvement. The three primary goals include low latency, high accuracy, and energy efficiency. Latency, or inference time, is critical because many IoT applications such as real-time video analytics, environmental sensing, or health monitoring require immediate responses to incoming data. High accuracy is equally important to ensure the system's reliability and effectiveness in decision-making, especially in safety-critical use cases like autonomous systems or medical devices. However, these objectives must also be balanced against energy consumption, as many edge devices operate on batteries or under stringent power budgets. Energy-efficient inference prolongs device lifetime, reduces maintenance costs, and enables deployment in remote or power-limited environments. Achieving an optimal trade-off between these goals especially when they are often conflicting is a central challenge in designing models for IoT edge computing.

3.2. Constraints Due to Hardware (Memory, Computation, Battery)

Edge devices come in a wide variety of hardware configurations, but they all share one common characteristic: resource constraints. Limited computational power means that deep learning models must run with reduced FLOPs (floating point operations per second) and without relying on high-end CPUs or GPUs typically available in cloud infrastructure. Memory constraints limit the model size, the number of activations stored during inference, and the batch size used during processing. For instance, many IoT devices may have less than 1 GB of RAM, which imposes a strict upper bound on the model complexity and data handling capabilities. Furthermore, battery life imposes an energy ceiling that models must

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stay within to ensure prolonged, uninterrupted operation. These hardware-level constraints not only shape the model design but also necessitate efficient deployment pipelines, specialized software stacks, and sometimes custom firmware to support real-time inference. Any neural network architecture intended for edge devices must be aware of and compatible with these constraints, making traditional large-scale models unsuitable for such deployments without significant adaptation.

3.3. Formal Problem Statement of NAS for Edge IoT

The goal of applying Neural Architecture Search in the context of IoT edge computing can be formally stated as a multi-objective constrained optimization problem. Given a defined search space A\mathcal{A}A of neural network architectures and a target hardware profile HHH, the objective is to find an architecture a∗∈Aa^* \in \mathcal{A}a∗∈A that maximizes predictive accuracy Acc(a)Acc(a)Acc(a), while minimizing latency Lat(a,H)Lat(a, H)Lat(a,H), model size Size(a)Size(a)Size(a), and energy consumption Energy(a,H)Energy(a, H)Energy(a,H), subject to hardware constraints CHC_HCH. Mathematically, this can be expressed as:
a∗=arg⁡max⁡a∈A Acc(a)subject toLat(a,H)≤Lmax, Size(a)≤Mmax, Energy(a,H)≤Emaxa^* = \arg\max_{a \in \mathcal{A}} \; Acc(a) \quad \text{subject to} \quad Lat(a, H) \leq L_{max}, \; Size(a) \leq M_{max}, \; Energy(a, H) \leq E_{max}a∗=arga∈AmaxAcc(a)subject toLat(a,H)≤Lmax ,Size(a)≤Mmax,Energy(a,H)≤Emax Where LmaxL_{max}Lmax, MmaxM_{max}Mmax, and EmaxE_{max}Emax are maximum acceptable thresholds for latency, model size, and energy consumption, respectively. This problem formulation emphasizes the need for NAS to search intelligently within the architecture space, guided not only by accuracy but also by hardware-aware constraints to ensure feasible and deployable solutions for real-world edge IoT devices.

4. NEURAL ARCHITECTURE SEARCH METHODOLOGY

4.1. Search Space Design: Types of Neural Layers and Operations Considered

The effectiveness of NAS heavily depends on the design of the search space, which defines the set of all possible architectures the search algorithm can explore. For edge devices, the search space must be carefully crafted to include lightweight operations that are computationally efficient. Typical components in such a space include depthwise separable convolutions, group convolutions, dilated convolutions, squeeze-and-excitation blocks, residual connections, and pointwise (1x1) convolutions. These elements are selected for their ability to reduce computation while retaining high representational power. In some frameworks, mobile-friendly modules such as Inverted Residual Blocks (used in MobileNetV2) or Ghost Modules are included. The search space may be structured hierarchically (e.g., cell-based NAS), where small blocks or cells are discovered and then stacked to form the complete architecture. This modular design not only reduces the computational burden during the search but also allows for architecture reuse and scalability. A well-designed search space ensures the discovered models are not only performant but also deployable on constrained edge hardware.

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4.2. Search Strategy: Reinforcement Learning, Evolutionary Algorithms, Gradient-Based Methods, or Hybrid

NAS employs various strategies to explore the search space and discover optimal architectures. One popular approach is Reinforcement Learning (RL), where a controller—often modeled as a recurrent neural network—generates candidate architectures and receives feedback based on their performance. The controller then learns to generate better architectures over time. Another widely used method is Evolutionary Algorithms (EA), which simulate natural selection processes by evolving a population of architectures through mutations and crossovers based on fitness (e.g., accuracy, latency). More recently, gradient-based NAS methods such as DARTS (Differentiable Architecture Search) have emerged, allowing for faster and more efficient search by relaxing the architecture space into a continuous domain and optimizing it using gradient descent. Hybrid approaches combine strengths of multiple strategies—for example, combining EA with weight-sharing or incorporating reinforcement learning within gradient-based frameworks—to accelerate search and improve robustness. For edge-specific NAS, strategies often integrate hardware feedback directly into the reward function or fitness evaluation to ensure resource-efficient architectures.

4.3. Objective Functions and Multi-Objective Optimization (Accuracy vs. Latency vs. Energy)

In NAS for edge computing, the search must balance multiple, often competing objectives, such as accuracy, latency, and energy consumption. This gives rise to multi-objective optimization, where the goal is to identify architectures that offer the best trade-offs. One common approach is to use Pareto optimization, where solutions are considered optimal if no other solution improves one objective without worsening another. Alternatively, some NAS methods formulate a single composite objective function, combining multiple metrics using weighted sums or penalty terms—for example:
Objective=Acc(a)−λ1·Lat(a)−λ2·Energy(a)\text{Objective} = Acc(a) - \lambda_1 \cdot Lat(a) - \lambda_2 \cdot Energy(a)Objective=Acc(a)−λ1·Lat(a)−λ2·Energy(a)
Here, λ1\lambda_1λ1 and λ2\lambda_2λ2 are hyperparameters that balance the trade-offs between performance and efficiency. Some approaches adaptively tune these weights based on real-time feedback or user preferences. In hardware-aware NAS, these objectives are not theoretical—they are measured using actual or simulated execution on target devices. This ensures that the selected architectures are not only optimal in theory but also practically viable on the intended hardware.

4.4. Dataset and Benchmarks Used for Evaluation

The evaluation of NAS-generated models requires suitable datasets and benchmark platforms to ensure the results are both valid and comparable. For image classification tasks, commonly used datasets include CIFAR-10, CIFAR-100, and ImageNet, with varying degrees of complexity and dataset sizes. CIFAR-10 and CIFAR-100 are useful for initial testing due to their small image sizes and manageable training costs, whereas ImageNet provides a more rigorous benchmark for assessing scalability and real-world applicability. For IoT-specific tasks, domain-specific datasets such as EdgeImpulse, TinyML datasets, or real-world sensor datasets may be used to reflect deployment conditions more accurately.

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Evaluation is typically performed both in simulation and on actual edge hardware platforms like Raspberry Pi, Jetson Nano, or STM32 microcontrollers. Key performance metrics include classification accuracy, inference latency (measured in milliseconds), energy consumption (in millijoules per inference), and model size (in megabytes or parameters). The combination of standard datasets and edge-specific benchmarks provides a robust framework for assessing the practicality and generalization ability of the discovered architectures.

5. IMPLEMENTATION AND EXPERIMENTAL SETUP

5.1. Description of IoT Edge Device(s) Used for Testing (e.g., Raspberry Pi, Microcontrollers)

To validate the effectiveness of the proposed NAS framework for edge computing, we conducted experiments on widely-used IoT edge devices that reflect typical resource constraints. The primary testing platform was the Raspberry Pi 4 Model B, equipped with a quad-core ARM Cortex-A72 CPU and 4 GB of RAM. This device is representative of general-purpose edge platforms used in home automation, surveillance, and industrial IoT applications. Additionally, we included a microcontroller-based device, the STM32F746G Discovery board, which features an ARM Cortex-M7 processor and operates with significantly tighter power and memory constraints. These platforms were selected to capture a broad spectrum of edge device capabilities—from moderately powerful edge nodes to deeply embedded, ultra-low-power microcontrollers. The diversity in hardware allowed us to test how well NAS-generated models adapt to different levels of computational and energy limitations, providing insight into the framework's portability and scalability across IoT use cases.

5.2. Training Procedure and NAS Search Process Details

The NAS framework was implemented using a search space consisting of lightweight convolutional blocks, including depthwise separable convolutions, inverted residual blocks, and pointwise convolutions, optimized for low-latency inference. We used a weight-sharing approach to speed up the search process, similar to ENAS (Efficient NAS), where all candidate architectures share weights from a supernet trained once. The NAS controller was trained using reinforcement learning, where the reward function incorporated both accuracy and latency feedback collected from the target hardware. The search phase was conducted on a workstation with an NVIDIA GPU for efficiency, while inference time and energy measurements were collected directly on the edge devices. After selecting the top-performing architectures based on the multi-objective criteria, the final models were retrained from scratch to ensure fair and unbiased performance evaluation. The training used stochastic gradient descent (SGD) with a cosine annealing learning rate schedule and data augmentation techniques like random cropping and horizontal flipping for robustness.

5.3. Evaluation Metrics (Accuracy, Inference Time, Power Consumption, Model Size)

To comprehensively assess the performance of the NAS-generated models, we used four key evaluation metrics: classification accuracy, inference latency, power consumption, and model size. Accuracy was measured as the top-1 classification accuracy on the test set of standard datasets such as

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CIFAR-10 and TinyImageNet. Inference latency was recorded using timestamps before and after model execution on the edge device, averaged over multiple runs to ensure consistency. Power consumption was monitored using external power measurement tools (e.g., USB digital multimeters or energy profilers) that recorded the device's current draw during inference. Model size was computed based on the total number of parameters and on-device memory footprint (in megabytes). These metrics collectively capture the trade-offs between performance and efficiency, enabling a rigorous comparison of NAS-generated models with baseline architectures in edge environments.

6. RESULTS AND ANALYSIS

6.1. Comparison of NAS-Designed Models with Baseline Models (e.g., MobileNet, TinyML Models)

The NAS-generated models were evaluated against several widely used lightweight neural network architectures, including MobileNetV2, ShuffleNet, and representative models from the TinyML community. Across various benchmarks and hardware configurations, the NAS-designed models consistently demonstrated superior trade-offs between accuracy and efficiency. For example, on the CIFAR-10 dataset, the NAS-discovered architecture achieved a top-1 accuracy of 91.4% while reducing inference latency on the Raspberry Pi by 25% compared to MobileNetV2. On microcontroller platforms like the STM32, the NAS model required 35% less memory and consumed 30% less energy than its manually designed counterparts. These results indicate that the automatic design process successfully tailored architectures to the hardware constraints, outperforming even highly-optimized human-designed models under real-world deployment scenarios.

6.2. Trade-Offs Observed Between Accuracy, Latency, and Energy

The experiments revealed important insights into the trade-offs involved in deploying deep learning models at the edge. While NAS was able to discover models with strong accuracy, achieving the absolute best accuracy often came at the cost of increased latency or energy consumption. Conversely, aggressively minimizing latency or power often led to slight reductions in accuracy. However, the multi-objective optimization framework allowed for effective navigation of these trade-offs, producing Pareto-optimal models that balance all critical objectives. These findings confirm that no single model dominates across all metrics, and that the "best" model often depends on the specific priorities of the application—whether it's maximizing battery life, minimizing response time, or maintaining high prediction reliability.

6.3. Ablation Studies on Different NAS Components or Configurations

To understand the contribution of different NAS components, we performed ablation studies by systematically varying elements of the search space and search strategy. For instance, removing hardware latency feedback from the reward function led to the discovery of architectures that were more accurate but significantly slower on the edge device, demonstrating the importance of real-time, hardware-in-the-loop evaluation. Similarly, replacing depthwise separable convolutions with standard convolutions in the search space increased model size and inference time, reinforcing the value of

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efficient layer choices. We also tested alternative search strategies (e.g., random search versus reinforcement learning) and found that guided search methods consistently yielded better performance. These ablation studies validate the core design choices of the NAS framework and highlight how each component contributes to overall performance in the edge computing context.

6.4. Discussion on Practical Deployment Feasibility

One of the most critical aspects of NAS research for IoT is ensuring that the designed models are practically deployable. Our deployment tests confirmed that the NAS-generated models could be integrated into real-time edge applications without requiring specialized hardware accelerators or excessive manual tuning. On Raspberry Pi, models ran within acceptable latency and power budgets, while on microcontrollers, the final models fit within flash memory and RAM constraints, enabling continuous inference in low-power settings. The ease of integration and consistent performance across platforms demonstrates the real-world applicability of the proposed framework. However, deployment challenges such as toolchain compatibility, quantization errors, and firmware limitations still exist and must be considered in future work.

7. DISCUSSION

7.1. Strengths and Limitations of the NAS Approach for IoT Edge Computing

The proposed NAS framework presents several notable strengths for edge computing. It eliminates the need for manual architecture design, reduces development time, and produces models that are well-adapted to the specific constraints of edge devices. The integration of hardware feedback during the search process ensures that the final models are not only accurate but also optimized for real-world deployment, which is a critical requirement in IoT systems. Furthermore, the modular and extensible nature of the search space allows for adaptation to different device capabilities and task domains. However, there are also limitations. The NAS search process, even when accelerated, remains computationally intensive, often requiring significant GPU resources during the search phase. Additionally, the current implementation assumes static hardware characteristics; variations in operating conditions or device heterogeneity are not fully addressed. Moreover, deploying NAS-generated models on deeply constrained devices like 8-bit microcontrollers still poses challenges in quantization and memory alignment, which were only partially mitigated in this work.

7.2. Potential Improvements and Future Research Directions (e.g., Federated NAS, Hardware-Aware NAS)

Looking forward, several promising research directions can enhance the utility and scalability of NAS for edge computing. One important avenue is Federated NAS, which distributes the search and training processes across multiple edge devices without requiring centralized data collection. This approach aligns well with privacy-preserving requirements in IoT networks and reduces the communication overhead with the cloud. Another area is the development of adaptive and online NAS frameworks that can dynamically adjust model architectures in response to changing hardware

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conditions, such as battery degradation or fluctuating workload patterns. Enhancing hardware-awareness further by incorporating detailed profiling of device-specific accelerators (e.g., DSPs, NPUs) could lead to even more efficient models. Finally, expanding NAS applications beyond classification to include tasks like object detection, time-series forecasting, or anomaly detection in edge environments will broaden its impact. By addressing these challenges, future NAS frameworks can become a foundational technology for building intelligent, responsive, and efficient IoT systems.

8. CONCLUSION

In this work, we presented a comprehensive study on the application of Neural Architecture Search (NAS) for optimizing deep learning model deployment on resource-constrained IoT edge devices. By addressing the core challenges posed by limited computational resources, energy constraints, and real-time latency requirements, our NAS framework was able to automatically discover neural network architectures that strike a favorable balance between accuracy, inference speed, and power consumption. Through careful search space design, integration of hardware-aware objective functions, and reinforcement learning-based search strategies, we demonstrated the effectiveness of NAS-generated models across a variety of IoT platforms including Raspberry Pi and microcontrollers. The experimental results showed that NAS can outperform manually designed lightweight architectures like MobileNet and TinyML baselines in both accuracy and efficiency metrics. Additionally, our ablation studies confirmed the critical role of multi-objective optimization and layer-level design decisions in influencing deployment feasibility. These findings have significant implications for the future of IoT edge computing, suggesting that NAS can be a foundational technology for enabling scalable, autonomous, and intelligent edge intelligence. The ability to generate custom, hardware-tailored architectures can drastically reduce the development cycle and enable broader adoption of machine learning in distributed and embedded systems. While the current study focuses on static hardware profiles, future work could explore dynamic or federated NAS to address heterogeneity and on-device adaptation. Overall, our results not only validate the potential of NAS as a tool for edge optimization but also open new avenues for research in the design of resource-aware learning systems in IoT ecosystems. As edge devices become more intelligent and autonomous, the role of NAS in driving this evolution is likely to become increasingly vital.

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